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A PCI Express Compliance Coverage Report Example

The following is a sample segment of the compliance coverage report from a regression run of the PCIE-VR compliance suite.

TX	RX	Covered Item
124412	592	PHY.02.02#01 Ordered-sets are always transmitted serially on each lane such that a full ordered set appears simultaneously on all lanes of a multi-lane link
6896	7777	PHY.02.02#02 The Framing mechanism uses Special Symbol K28.2 'SDP' to start a DLLP.
7306	7471	PHY.02.03#01 TLPs must be framed by placing an STP Symbol at the start of the TLP and an END Symbol or EDB Symbol at the end of the TLP
6896	7777	PHY.02.03#02 DLLPs must be framed by placing an SDP Symbol at the start of the DLLP andan END Symbol at the end of the DLLP
294	294	DLL.02.01#16 While in DL_Init and state FC_INIT1, report DL_Down status
4978	4978	DLL.02.01#17 While in DL_Init and in state FC_INIT2, report DL_Up status
98	98	DLL.02.01#18 While in DL_Init, exit to DL_Active if: Flow Control initialization Completes uccessfully and the Physical Layer continues to report hysical LinkUp = 1.
96	96	DLL.02.01#21 While in DL_Active, exit to DL_Inactive if Physical Layer reports physical linkUp = 0.
294	294	DLL.03.01#02 For any VC1-7, while in FC_INIT1, all TLPs for that VCx are blocked by the transaction layer
98	98	DLL.03.01#03 For VC0, while in FC_INIT1, uninterrupted ordered triplets of IntiFC1 DLLPs must be sent at the maximum rate possible on the Link
98	98	TPL.03.04#06 Each enabled Switch Port must comply with the flow control rules as listed in the Base Specification
1650	7306	TXN.02.01#01 All Transaction Layer Packet headers must follow the field format specified in Figure 2-4 of the Base Specification.
1650	7306	TXN.02.01#02 Permitted Fmt[1:0] and Type[4:0] field values are shown in Table 2-3 of the Base Specification. All other encodings are reserved.
1650	7306	TXN.02.01#03 TD Field u 1b indicates presence of TLP digest in the form of a single DW at the end of the TLP.
1650	3674	TXN.02.01#04 TLP data must be four-byte naturally aligned and in increments of four-Byte Double Words.
1650	2824	CFG.08.04#12 A device must not generate TLPs exceeding the Max_Payload_Size.
91	455	PMG.01.01#01 Root complexes are required to participate in Link power management DLLP protocols initiated by the downstream device.